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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,047	10/30/2003	Ji-young Kim	9898-300	1200

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EXAMINER	
DUONG, KHANH B	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 09/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,047	KIM, JI-YOUNG	
	Examiner	Art Unit	
	Khanh B. Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 30, 2006 has been entered.

Response to Amendment

Accordingly, claims 8 and 20 were amended, and new claims 25 and 26 were added.

Currently, claims 8-15 and 17-26 remain pending.

Response to Arguments

Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection under Tabata et al. (US 2006/0035434 A1), Weis and Ishikawa.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 8-15 and 17-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Re claims 8, 20 and 25, the amended claims recite "simultaneously patterning the capping layer and the gate conductive layer". This limitation was not described in the specification. The specification states at page 2, paragraph 0024, that the capping layer and the gate conductive layer are "successively patterned". Please note that the terms "simultaneously" and "successively" do not have the same meaning as the former means "existing at the same time" and the latter means "following in order" [see Merriam-Webster Online Dictionary].

*** Other claims are rejected as depending on the rejected base claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 8, 11-15, 17, 19, 20 and 22-26 are rejected, as understood, under 35 U.S.C. 103(a) as being unpatentable over Weis (US 2002/0196651 A1) in view of Tabata et al. (US 2006/0035434 A1).

Weis discloses in FIG. 2 a method of forming a MOSFET having a recessed channel, comprising: forming a trench in a semiconductor substrate using a etch process; forming a gate dielectric layer (32 and 36) on an inner wall and a bottom of said trench; sequentially forming a gate conductive layer 34 and a capping layer 44 on the gate dielectric layer so as to fill the trench; forming a gate electrode having a first portion (portion of 34 over the substrate) which rises over the semiconductor substrate and a second portion (in the substrate) filling the trench by patterning the capping layer 44 and the gate conductive layer 34, wherein the first portion has a smaller width than that of the second portion; forming spacers 46 on the sidewalls of the gate electrode 34, wherein a portion of the spacers 46 are extended into the semiconductor substrate; and forming a source/drain region 38 by implanting impurity ions into the semiconductor substrate on both sides of the gate electrode 34, and wherein forming the gate electrode 34 comprises recessing the gate conductive layer that fills the trench to a depth of approximately 70 nm (700 Angstroms) from a top surface of the semiconductor substrate by inherently adjusting etching time.

Re claim 8, Weis does not disclose successively patterning the capping layer and the gate conductive layer.

Tabata et al. ("Tabata") suggests in FIGs. 13-15 successively patterning a capping layer (13, 14) and a gate conductive layer (7, 10, 12) for the purpose of forming a strip pattern extending across the upper portions of the trenches 4 similarly to a photoresist film 41 [see page 4, paragraph 0070].

Since Weis and Tabata are from the same field of endeavor, the purpose disclosed by Tabata would have been recognized in the pertinent prior art of Weis.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Weis as suggested by Tabata because of the desirability to form a strip pattern extending across the upper portions of the trenches similarly to the photoresist film.

Re claim 11, Weis discloses the gate dielectric layer (32 and 36) is formed of silicon oxide [see page 2, paragraphs 0023 and 0024].

Re claim 12, Weis discloses the gate conductive layer comprises a conductive polysilicon layer 34 that fills the trench and a metal layer (40 and 42) formed on the conductive polysilicon layer 34 [see pages 2-3, paragraph 0024].

Re claim 13, Weis discloses in FIGs. 4a and 4b forming a sacrificial (collar) oxide layer 30 by thermally oxidizing the semiconductor substrate; and removing the sacrificial oxide layer 30 using a wet etch process [see page 3, paragraph 0028].

Re claim 14, Weis discloses recessing the gate conductive layer that fills the trench to a depth of approximately 70 nm (700 Angstroms), instead of 500 Angstroms or less from the surface of the semiconductor substrate.

However, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select an appropriate depth. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed

produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Re claims 15 and 17, Weis expressly discloses in FIG. 2 forming spacers (parts of 44 and 46) on sidewalls of the gate electrode (34, 40, 42 and 44), wherein a portion of the spacers (parts of 46) are extended into the semiconductor substrate.

Re claim 19, Weis expressly discloses in FIG. 2 the source/drain region 38 is shallower than the bottom of the trench.

Re claim 20, see discussions above regarding claims 8 and 14.

Re claim 22, Weis expressly discloses in FIG. 2 the source/drain region 38 is shallower than the bottom of the trench.

Re claims 23 and 24, Weis expressly discloses in FIG. 2 the width of the first portion of the gate electrode 34 plus the spacers 46 is less than that of the second portion of the gate electrode 34, and that the spacers 46 extend the entire height of the first portion of the gate electrode.

Re claims 25 and 26, see discussions above regarding claims 8 and 14. Sabata further teaches in FIG. 12 forming the capping layer (13, 14) is performed immediately after forming the gate conductive layer (7, 10, 12).

Claims 9, 10, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weis and Tabata as applied to claims 8, 11-15, 17, 19, 20 and 22-26 above, and further in view of Ishikawa et al. (US 6,482,701).

Re claims 9, 10, 18 and 21, Weis and Tabata fail to disclose the specific depth of the trench of about 1000 Angstroms to about 1500 Angstroms and further etching the trench by about 100 Angstroms to about 200 Angstroms using a chemical dry etch process.

Ishikawa teaches in FIGs. 1A-1D a rectangular trench 5 is formed to a depth of about 4 to 6 micrometers (40,000 to 60,000 angstroms) and is further etched to about 0.10 to 0.20 micrometers (1,000 to 2,000 angstroms) using a chemical dry etch process.

Since Weis, Tabata and Ishikawa are from the same field of endeavor, the purpose disclosed by Ishikawa would have been recognized in the pertinent prior art of Weis and Tabata.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined method of Weis and Tabata in the manner as taught by Ishikawa, since Ishikawa states at column 1, lines 35-48 that such modification would reduce not only deterioration in film quality or thinning of a gate oxide, but also electric field at the corner of a bottom portion of the trench. As a result, a withstand voltage breakdown would be minimized at such corner.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Luo (US 6,251,730) and Dyer (US 6,518,616) disclose relevant information regarding methods of forming a MOSFET having a recessed channel.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KBD

Zandra V. Smith
Supervisory Patent Examiner
5 Sept 2006